

PROGRAMMABLE OVERVOLTAGE PROTECTOR

DESCRIPTION:



The ALPSVG170Q is especially designed for short loop system. It can be independent tracking overvoltage protection for two SLICs (Subscriber Line Interface Circuit). Positive over voltages are clipped to common by forward conduction of this device antiparallel diode. Negative over voltages are initially clipped close to the SLIC negative supply by emitter follower action of this buffer transistor.

FEATURES:

- Dual voltage-programmable protector
- Supports battery voltages down to -167 V
- Low gate triggering current 5 mA max.
- High holding current 150 mA min.
- Specified 2/10 limiting voltage
- ESD Immunity (HBM): JESD22 Class 3B, $\geq 8\text{KV}$
- MLS: Lever 1 - unlimited

APPLICATIONS:

- Wireless In the Local Loop (WILL)
- Fibre In The Loop (FITL)
- Digital Added Main Line, Pair Gain (DAML)
- Small Office Home Office (SOHO)
- Integrated Services Digital Network – Terminal Adaptors (ISDN-TA)

MAXIMUM RATINGS

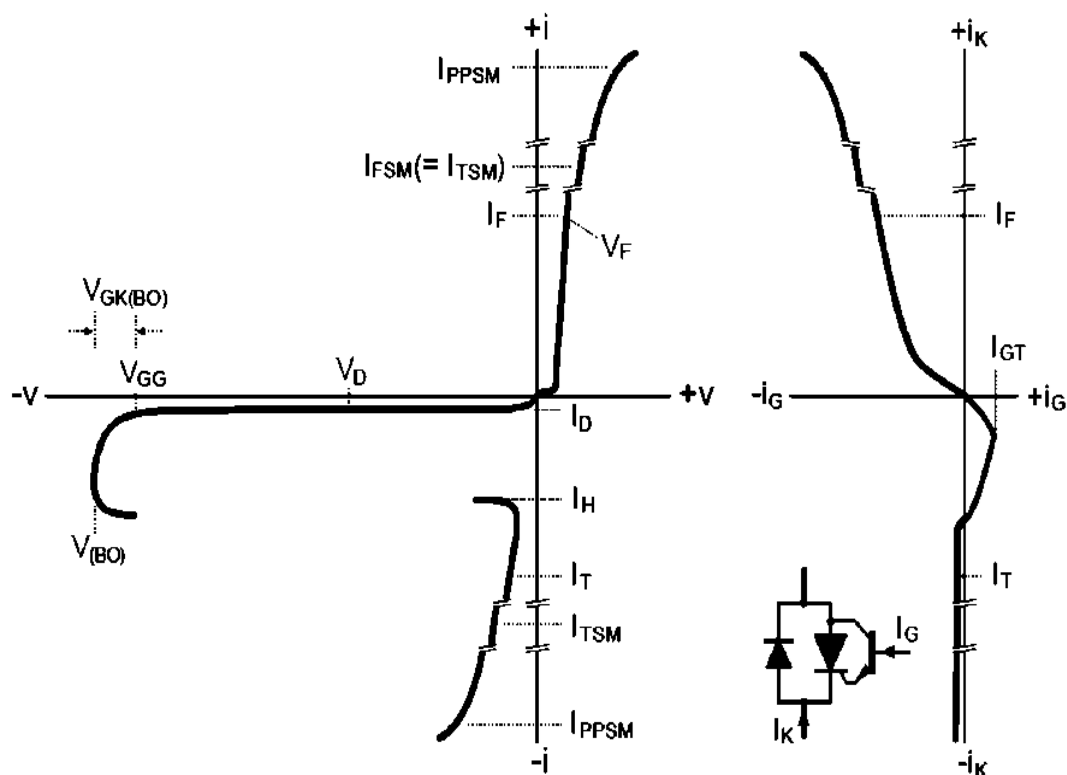
MAXIMUM RATINGS @ $T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise specified			
PARAMETER	SYMBOL	RATINGS	UNIT
Non-repetitive peak impulse current ^(1, 2) 10/1000 μS (Telcordia GR-1089-CORE) 5/310 μS (ITU-T K.20, K.21, K.45, K.44 wave shape 10/700s) 2/10 μS (Telcordia GR-1089-CORE)	I_{PPSM}	30 40 120	A
Non-repetitive peak on-state current, 50 Hz / 60 Hz ^(1, 2, 3) 0.5s 1s 5s 30s 900s	I_{TSM}	6.5 4.5 2.4 1.3 0.72	A
Non repetitive peak gate current, 1/2 μs pulse, cathodes commoned	I_{GSM}	40	A
Repetitive peak off-state voltage, $V_{\text{GK}} = 0$	V_{DRM}	-170	V
Repetitive peak gate-cathode voltage, $V_{\text{KA}} = 0$	V_{GKRM}	-167	V
Operating free-air temperature range	T_A	-40 to +85	$^{\circ}\text{C}$
Operating Junction Temperature	T_J	-40 to +150	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-40 to +150	$^{\circ}\text{C}$
Maximum lead temperature for soldering during 10s	T_L	260	$^{\circ}\text{C}$
Junction to free air thermal resistance ⁽⁴⁾	$R_{\theta\text{JA}}$	120	$^{\circ}\text{C/W}$
Note: 1. Initially the device must be in thermal equilibrium with $T_J = 25\text{ }^{\circ}\text{C}$. The surge may be repeated after the device returns to its initial conditions. 2. The rated current values may be applied to either of the Line to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of a single terminal pair). 3. Values for $V_{\text{GG}} = -100\text{ V}$ 4. EIA/JESD51-3 PCB, EIA/JESD51-2 environment, $\text{PTOT} = 1.7\text{ W}$			

ELECTRICAL CHARACTERISTICS @ TA = 25 °C unless otherwise specified

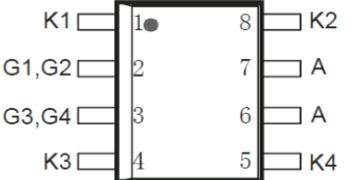
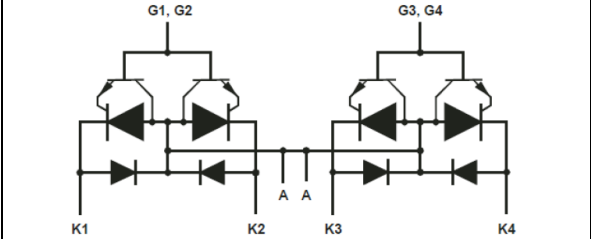
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Forward Voltage	$I_F=5A$, $t_w=200\mu s$	V_F			3	V
Ramp peak forward recovery voltage	$di/dt=\pm 10A/\mu s$, $dv/dt\leq\pm 100V/\mu s$ maximum ramp value= $\pm 10A$, $T_J=25^\circ C$	V_{FRM}			5	V
Impulse peak forward recovery voltage	$2/10\mu s$, $I_{TM}=-27A$, $R_s=50\Omega$, $di/dt=27A/\mu s$	V_{FRM}			12	V
Off-state current	$V_D=V_{DRM}$, $V_{GK}=0$ $T_J=25^\circ C$	I_D			-5	μA
Ramp Breakover voltage	$di/dt=\pm 10A/\mu s$, $dv/dt\leq\pm 100V/\mu s$, $V_{GG}=-100V$ maximum ramp value= $\pm 10A$, $T_J=25^\circ C$	$V_{(BO)}$			-112	V
Impulse breakover voltage	$2/10\mu s$, $I_{TM}=-27A$, $R_s=50\Omega$, $di/dt=-27A/\mu s$, $V_{GG}=-100V$	$V_{(BO)}$			-115	V
Gate-cathode impulse breakover voltage	$2/10\mu s$, $I_{TM}=-27A$, $R_s=50\Omega$, $di/dt=-27A/\mu s$, $V_{GG}=-100V$	$V_{GK(BO)}$			15	V
Holding current	$I_T=-1A$, $di/dt=1A/ms$, $V_{GG}=-100V$	I_H	-150			mA
Gate reverse current	$V_{GG}=V_{GK}=V_{GKRM}$, $V_{KA}=0$ $T_J=25^\circ C$	I_{GKS}			-5	μA
Gate trigger current	$I_T=-3A$, $t_{p(g)}\geq 20\mu s$, $V_{GG}=-100V$ $T_J=25^\circ C$	I_{GT}			5	mA
Gate-Cathode trigger voltage	$I_T=-3A$, $t_{p(g)}\geq 20\mu s$, $V_{GG}=-100V$	V_{GT}			2.5	V
Anode-cathode offstate capacitance	$f=1MHz$, $V_d=1V$, $I_G=0$ $V_D=-3V$ $V_D=-48V$	C_{AK}			100 55	pF

PARAMETER MEASUREMENT INFORMATION

Parameter	Symbol
Off-state current	I_D
Holding current	I_H
Breakover voltage	$V_{(BO)}$
Forward voltage	V_F
Peak forward recovery voltage	V_{FRM}
Gate-cathode impulse breakover voltage	$V_{GK(BD)}$
Gate reverse current	I_{GKS}
Gate trigger current	I_{GT}
Gate-cathode trigger voltage	V_{GT}
Cathode-anode off-state capacitance	C_{KA}

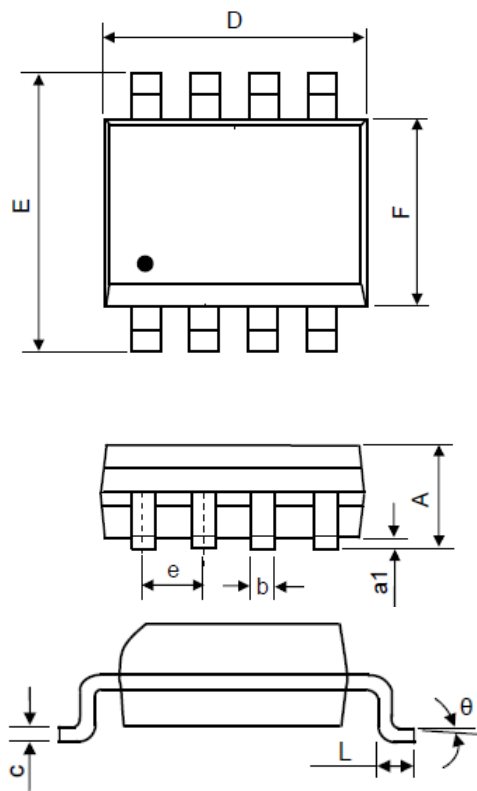


PINNING INFORMATION

PIN CONFIGURATION	SIMPLIFIED OUTLINE	SCHEMATIC DIAGRAM
K1, K3, K4, K2 - Connect to subscriber lines (Tip/Ring) G1, G2, G3, G4 - Connect to battery (Reference Voltage) A - Connect ground		

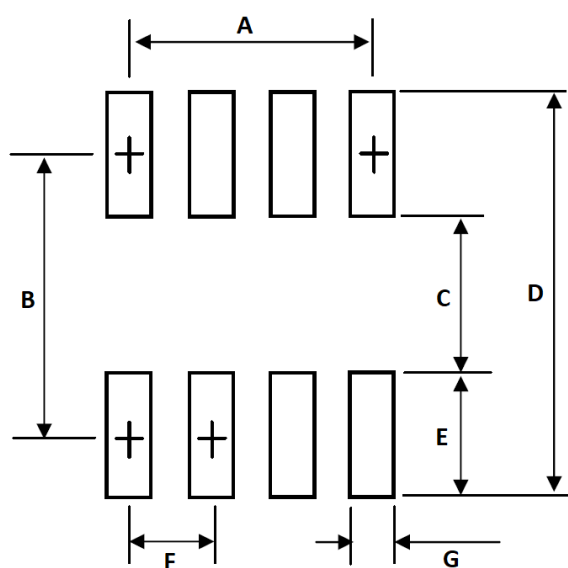
PACKAGE INFORMATION

SOP-8



OUTLINE DIMENSIONS		
SYMBOL	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
a1	0.10	0.25
D	4.80	5.20
E	5.80	6.20
F	3.80	4.00
b	0.33	0.51
e	1.27BSC	
c	0.17	0.25
L	0.40	1.27
θ	0°	8°

SUGGESTED SOLDER PAD LAYOUT



OUTLINE DIMENSIONS	
SYMBOL	MILLIMETERS
A	3.81
B	5.20
C	3.00
D	7.40
E	2.20
F	1.27
G	0.60

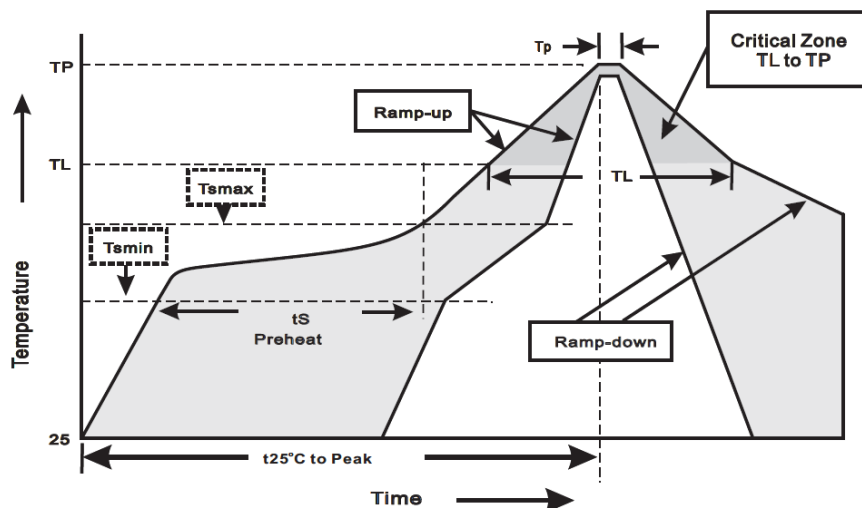
Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$
3. The pad layout is for reference purposes only.

SOLDERING PARAMETERS

SUGGESTED THERMAL PROFILES FOR SOLDERING PROCESSES

1. Storage environment: Temperature=5 °C~40 °C Humidity=55% ±25%
2. Reflow soldering of surface-mount devices



3. Reflow soldering

PROFILE FEATURE	SOLDERING CONDITION
Average ramp-up rate (T_L to T_P)	<3 °C/sec
Preheat	
- Temperature Min (T_{smin})	150 °C
- Temperature Max (T_{smax})	200 °C
- Time (min to max) (t_s)	60 ~ 120 sec
T_{smax} to T_L	
- Ramp-upRate	<3 °C/sec
Time maintained above:	
- Temperature (T_L)	217 °C
- Time(t_L)	60 ~ 260 sec
Peak Temperature (T_P)	255 °C-0/+5 °C
Time within 5 °C of actual Peak Temperature(t_P)	10 ~ 30 sec
Ramp-down Rate	<6 °C/sec
Time 25 °C to Peak Temperature	<6 minutes



beyond boundaries...

ALPSVG170Q

SOP-8

CUSTOMER NOTE:

DISCLAIMER

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2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).



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