PROGRAMMABLE OVERVOLTAGE PROTECTOR

DESCRIPTION:

The ALPSVG110S is a programmable overvoltage protection device designed to protect modern dual polarity supply rail ringing SLICs (Subscriber Line Interface Circuits) against over voltages on the telephone line. Over voltages can be caused by lightning, AC power contact and induction. Four separate protection structures are used; two positive and two negative to provide optimum protection during Metallic (Differential) and Longitudinal (Common Mode) protection conditions in both polarities. Dynamic protection performance is specified under typical international surge waveforms from Telcordia GR-1089-CORE, ITU-T K.44 and YD/T 950.

FEATURES:

- High Performance Protection for SLICs
- Wide Programming Range (-110V to +110V)
- Low gate triggering current 5 mA max
- Surge capability does not degrade after multiple surge events within its ratings
- High holding current 150mA min
- RoHS Compliant

APPLICATIONS:

- Wireless In the Local Loop (WLL)
- Voice applications which require regenerated POTS
- VoIP applications
- PBX
- FXS applications
- Digital Pair Gain systems (DPG)
- Digital Loop Carrier systems (DLC)
- Small Office Home Office (SOHO)

MAXIMUM RATINGS

MAXIMUM RATINGS @ T_A = 25 °C unless otherwise specified			
PARAMETER	**SYMBOL**	**RATINGS**	**UNIT**
Non-repetitive peak impulse current [1, 2, 3 ,4] 10/1000µS (Telcordia GR-1089-CORE) 5/310µS (ITU-T K.20, K.21, K.45, K.44 wave shape 10/700s) 2/10µS (Telcordia GR-1089-CORE)	I_{PPSM}	 ±30 ±68 ±100	A
Non-repetitive peak on-state current, 50 Hz / 60 Hz [1, 2, 3, 5] 0.2s 1s 900s	I_{TSM}	 9.0 5.0 1.7	A
Repetitive peak off-state voltage $V_{G1(Line)}$ = 0, V_{G2} ≥ +5 V $V_{G2(Line)}$ = 0, V_{G1} ≥ -5 V	V_{DRM}	 -120 +120	V
Maximum negative battery supply voltage	V_{G1M}	-110	V
Maximum positive battery supply voltage	V_{G2M}	+110	V
Maximum differential battery supply voltage	△V(BAT)M	220	V
Operating Junction Temperature	T_J	-40 to +150	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Thermal Resistance Junction to Ambient [6]	$R_{\theta JA}$	55 (Typ.)	°C/W

Note:

1. Initially the device must be in thermal equilibrium with T_J = 25 °C. The surge may be repeated after the device returns to its initial conditions.
2. The rated current values may be applied to either of the Line to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of a single terminal pair.
3. Rated currents only apply if pins 6 & 7 (Ground) are connected together.
4. Applies for the following bias conditions: V_{G1} = -20 V to -110 V, V_{G2} = 0 V to +110 V.
5. EIA/JESD51-2 environment and EIA/JESD51-7 high effective thermal conductivity test board (multi-layer) connected with 0.6 mm printed wiring track widths.
6. EIA/JESD51-2 Environment, PTOT = 4W, EIA/JESD51-7 high effective thermal conductivity test board (multi-layer) connected with 0.6 mm printed wiring track widths.

ELECTRICAL CHARACTERISTICS @ TA = 25 °C unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Off-state current	$V_D = V_{DRM}$, $V_{G1(Line)} = 0$, $V_{G2} \geq +5$ V $T_A = 25℃$ $T_A = 85℃$	I_D			 -5 -50	µA
	$V_D = V_{DRM}$, $V_{G2(Line)} = 0$, $V_{G1} \geq -5$ V $T_A = 25℃$ $T_A = 85℃$				 +5 +50	
Negative-gate leakage current	$V_{G1(Line)}$ = -220 V	$I_{G1(Line)}$			-5	µA
Positive-gate leakage current	$V_{G2(Line)}$ = +220 V	$I_{G2(Line)}$			+5	µA
Gate-Line impulse breakover voltage	V_{G1}= -100V, I_T= -100 A [7] 2/10 µs V_{G1}= -100V, I_T= -30 A 10/1000µs	$V_{G1L(BO)}$			-15 -11	V
Gate-Line impulse breakover voltage	V_{G1}= +100V, I_T= +100 A [7] 2/10 µs V_{G1}= +100V, I_T= +30 A 10/1000µs	$V_{G2L(BO)}$			+15 +11	V
Negative holding current	V_{G1}= -60 V, I_T= -1A, di/dt= 1A/ms	I_H-	-150			mA
Negative-gate trigger current	I_T = -5A, tp(g) ≥ 20µs, V_{G1} = -60V	I_{G1T}			+5	mA
Positive-gate trigger current	I_T = +5A, tp(g) ≥ 20µs, V_{G2} = 60V	I_{G2T}			-5	mA
Line – Ground off-state capacitance	f = 1MHz, VD = -3V, G1 & G2 open circuit	C_O		32		pF

TYPICAL DEVICE RATING AND CHARACTERISTICS CURVES (T_A = 25 °C unless otherwise noted)

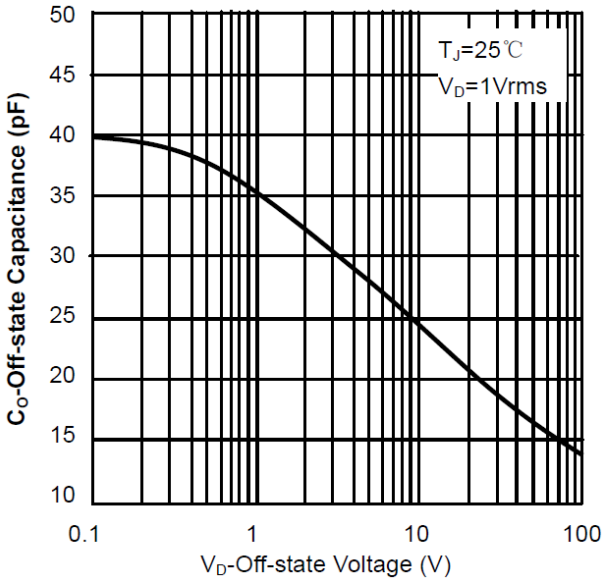


Fig.1 OFF-STATE CAPACITANCE VS OFF-STATE VOLTAGE

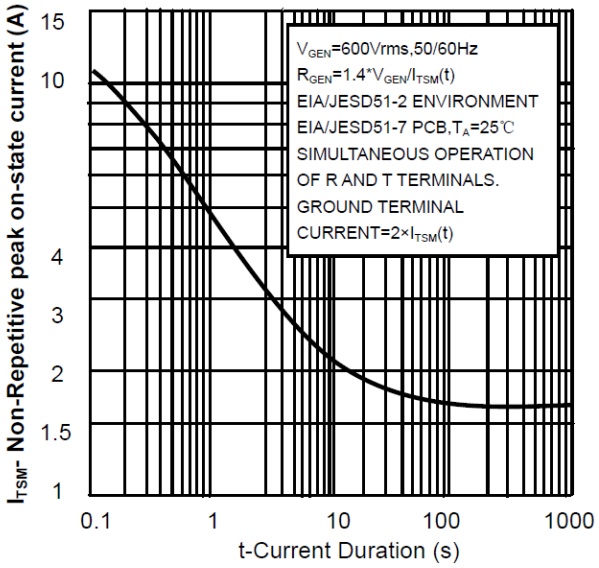
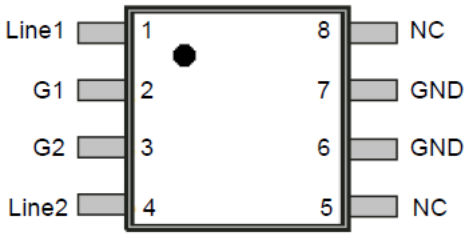
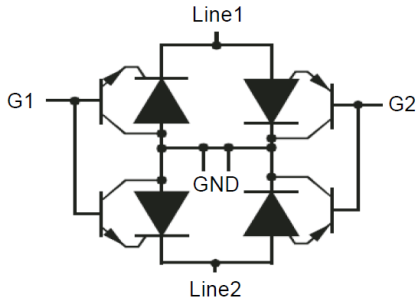


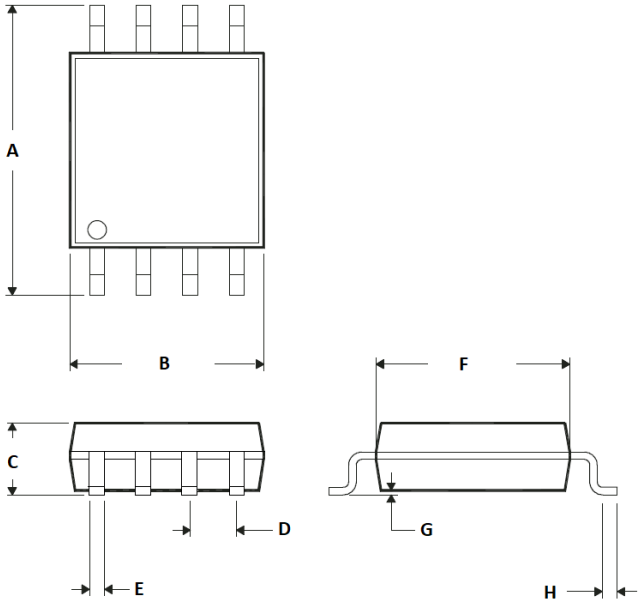
Fig.2 NON-REPETITIVE PEAK ON-STATE CURRENT VS CURRENT DURATION

PINNING INFORMATION

SIMPLIFIED OUTLINE	SCHEMATIC DIAGRAM
	

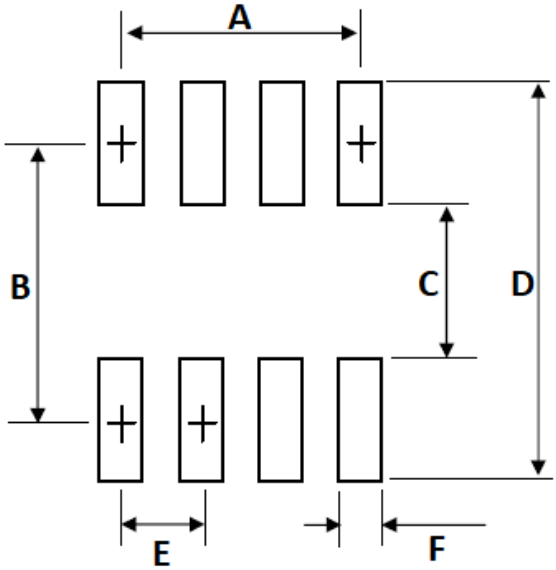
PACKAGE INFORMATION

8-SOIC



OUTLINE DIMENSIONS		
SYMBOL	MILLIMETERS	
	MIN	MAX
A	7.40	8.20
B	5.00	5.60
C	2.20 Max.	
D	1.27 Typ.	
E	0.35	0.51
F	5.00	5.60
G	0.10 Min.	
H	0.66 Typ.	

SUGGESTED SOLDER PAD LAYOUT



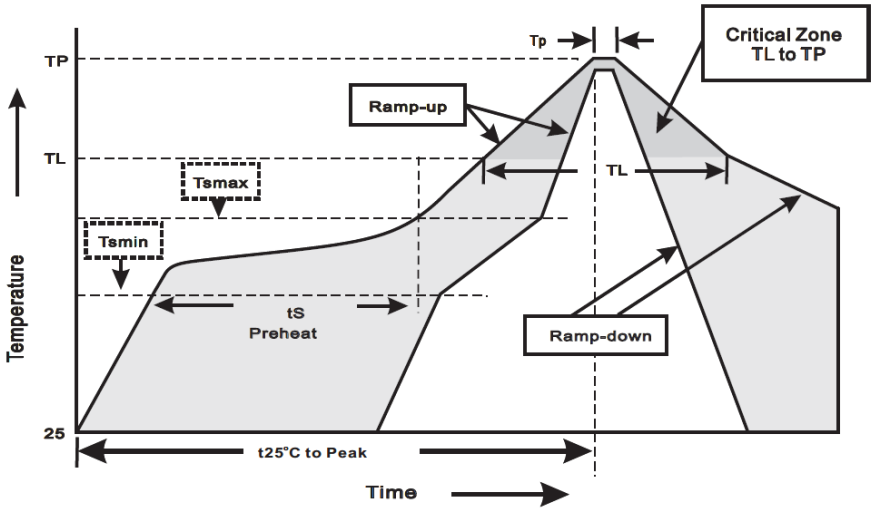
OUTLINE DIMENSIONS	
SYMBOL	MILLIMETERS
A	3.81
B	7.00
C	4.80
D	9.20
E	1.27
F	0.60

Note:
1. Controlling dimension: in millimeters.
2. General tolerance: ±0.05mm
3. The pad layout is for reference purposes only.

SOLDERING PARAMETERS

SUGGESTED THERMAL PROFILES FOR SOLDERING PROCESSES

1. Storage environment: Temperature=5 °C~40 °C Humidity=55% ±25%
2. Reflow soldering of surface-mount devices



3. Reflow soldering

PROFILE FEATURE	SOLDERING CONDITION
Average ramp-up rate (T_L to T_P)	<3 °C/sec
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (min to max) (t_s)	 150 °C 200 °C 60 ~ 120 sec
T_{smax} to T_L - Ramp-upRate	 <3 °C/sec
Time maintained above: - Temperature (T_L) - Time(tL)	 217 °C 60 ~ 260 sec
Peak Temperature (T_P)	255 °C-0/+5 °C
Time within 5 °C of actual Peak Temperature(tP)	10 ~ 30 sec
Ramp-down Rate	<6 °C/sec
Time 25 °C to Peak Temperature	<6 minutes

CUSTOMER NOTE:

DISCLAIMER

The product information and the selection guide facilitates the selection of the ALPINESEMI™'s Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review the Data sheet(s) so as to confirm that the Device(s) meets functionality parameters for your application. The information furnished on the Data Sheet and the ALPINESEMI™'s Web Site is believed to be accurate and reliable at the time of preparation of this document. ALPINESEMI™ however, does not assume any inaccuracies that may arise when the components are mounted and removed. Furthermore, ALPINESEMI™ does not assume liability whatsoever, arising out of the application or the use of any of ALPINESEMI™'s product(s). Neither, does it convey any license under its patent rights nor the rights of others. These products are not guaranteed for use in life saving/support appliances or systems. ALPINESEMI™'s customers using these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and ALPINESEMI™ will not be responsible in any way(s) for any damage(s) resulting from such use.

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2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

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